Amendments to specification:

Please amend the title, as follows:

--DRIVING CIRCUIT FOR FLAT DISPLAY PANEL ~~DISPLAYS~~--.

Please amend the indicated paragraphs of the original specification in accordance with the following particulars:

Page 2, lines 14 to line 17:

The primary object of the present invention is to provide a driving circuit for a flat display panel ~~for flat panel displays and a driving circuit disposed on the panel~~ to decrease the number of the parasitic capacitances on video lines so as to improve picture quality and to decrease power consumption.

Page 2, line 18 to Page 3, line 3:

To attain the above-mentioned object, a driving circuit for a flat display panel ~~displays disposed on a panel~~ according to the present invention comprises a plurality of video signal lines for providing analogous video signals, at least one buffer unit for inverting a scanning signal, and a plurality of switch units disposed between the video signal lines. Each of the switch units is connected to one of the video signal lines to receive an analogous video signal, and also, is connected to the output terminal of the buffer unit. A scanning signal enables the operation of the plurality of switch units so that a video signal is outputted to the display area (active area) ~~active area (display area)~~ of the flat ~~panel~~ display panel.

Page 3, lines 4 to 24:

The disposition between the plurality of switch units of the driving circuit and the display area ~~active area (display area)~~ of the flat panel display panel according to the present invention is not specifically defined. Preferably, the plurality of switch units and the display area ~~active area (display area)~~ of the flat ~~panel~~ display panel are spaced apart with at least one video signal line. The disposition of the video signal lines of the driving circuit according to the present invention is not specifically defined. Preferably, at least one video signal line is disposed between the switch units and the buffer unit for inverting a scanning signal. The disposition between the video signal lines and the switch units of the driving circuit according to the present invention is not specifically defined. Preferably, the video signal lines are disposed between the switch units and the display area ~~active area (display area)~~. The buffer unit for inverting a scanning signal of the driving circuit according to the present invention is not specifically defined. Preferably, the buffer unit for inverting a scanning signal is an amplification circuit, and more preferably, an inverting amplification circuit, to receive a timing signal, and then, amplify the timing signal to output at least one scanning signal. The flat ~~panel~~ display panel adapted to the driving circuit according to the present invention is not specifically defined. Preferably, the flat ~~panel~~ display panel is an organic light-emitting diode (OLED) display, or a liquid crystal display (LCD). Specifically, the LCD is the most preferred.

Page 4, line 19 to Page 5, line 3:

With reference to Fig. 2a, a schematic diagram of a driving circuit for sample/sustenance according to the first embodiment of the present invention is

shown. The circuit comprises a plurality of video signal lines 211, 212, 213, a plurality of switch units 221, 222, 223, a buffer unit for inverting a scanning signal 231 and ~~an active area (display area)~~ a display area (an active area) 241. The plurality of video signal lines 211, 212, 213 supply analog video signals; for example, the video signal line 211 supplies an analog video signal for blue, the video signal line 212 supplies an analog video signal for red, and the video signal line 213 supplies an analog video signal for green.

Page 5, lines 15 to Page 6, line 3:

In this embodiment, the plurality of switch units 221, 222, 223 can be of any electronic switches, and preferably, transistors, and more preferably, thin film transistors (TFTs). The plurality of switch units 221, 222, 223 are disposed between the video signal line 212 and the video signal line 213. Each n-type control gate of the switch units 221, 222, 223 is connected to the input terminal of the buffer unit and each p-type control gate of the switch units 221, 222, 223 is connected to the output terminal of the buffer unit 231. The switch units 221, 222, 223 are connected to the video signal lines 211, 212, 213 respectively. The scanning signals control the output of the plurality of switch units 221, 222, 223. With the arrival of the scanning signals, the plurality of switch units 221, 222, 223 output the video signals to data lines (not shown) in the active area (display area) 241 through output video signal lines 2211, 2221, 2231.

Page 6, lines 5 to Page 7, line 3:

Fig. 2b shows a schematic diagram of the parasitic capacitances associated with the first embodiment of the present invention. The parasitic

capacitance per pixel length on the video line 211 comes from crossover points 411, 412, 413 (as denoted in the three triangles in Fig. 2b) where the signal line wire intersects the video signal line 212 and lines 2311, 2312 connecting the buffer unit 231 and the plurality of switch units 221, 222, 223. The parasitic capacitance per pixel length on the video lines 212 comes from crossover points 421, 422, 423 (as denoted in the three squares in Fig. 2b) where the signal line wire intersects the buffer unit 231 and the lines 2311, 2312 connecting the plurality of switch units 221, 222, 223. The parasitic capacitance per pixel length on the video line 213 comes from crossover points 431, 432, 433 (as denoted in the three hexagons in Fig. 2b) where the signal line wire intersects the output signal lines 2211, 2221, 2231 of the plurality of switch units 221, 222, 223. Therefore, within a pixel length each video line has a parasitic capacitance from three crossover points for this embodiment. Figure 3a shows a schematic diagram of the driving circuit for sample/sustenance according to the second embodiment of the present invention. The components and the line connections of the second embodiment are similar to those of the first embodiment, except a plurality of switch units 321, 322, 323 disposed between a video signal line 313 (for providing an analogous video signal for green) and a video signal line 311 (for providing an analogous video signal for blue) as well as two video signal lines 311, 312 used to space the plurality of switch units 321, 322, 323 from ~~an active area (display area)~~ a display area 341.

Page 7, lines 4 to Page 7, line 18:

Fig. 3b shows a schematic diagram of the parasitic capacitances associated with the second embodiment of the present invention. The parasitic capacitance per pixel length on the video line 311 is due to crossover points 451,

452, 453, 454 (as denoted in four triangles in Fig. 3b) where the signal line wire intersects output signal lines 3211, 3221, 3231 of the plurality of switch units 321, 322, 323 and a line 3222 connecting the switch unit 322 to the video signal line 312. The parasitic capacitance per pixel length on the video line 312 is due to crossover points 461, 462, 463, 464 (as denoted in four hexagons in Fig. 3b) where the signal line wire intersects the output signal lines 3211, 3221, 3231 of the plurality of switch units 321, 322, 323 and the video signal line 311. The parasitic capacitance per pixel length on the video line 313 is due to crossover points 441, 442 (as denoted in two squares in Fig. 3b) where the signal line wire intersects lines 3311, 3312 connecting the buffer unit 331 and the plurality of switch units 321, 322, 323.